

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~striketrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 5-9, 13, 17, 21-25, 29, 43, and 47-50; please CANCEL claims 2-4, 10-12, 14-16, 18-20, 26-28, 30-32, 44-46, and 51-58 without prejudice or disclaimer; and please ADD claims 64-69 in accordance with the following:

1. **(Currently Amended)** A method to modulate address data of a disc type recording medium, the method comprising:

- generating the address data;
- performing error correction coding of the address data and outputting coded address data;
- receiving the coded address data ~~in a unit of at least two bits; and~~
- ~~generating a first modulated signal of the coded address data using a first modulation technique;~~
- ~~generating a second modulated signal of the coded address data using a second modulating signal; and~~
- generating a unit wobble signal of the coded address data by synthesizing the first and second modulated signals.

wherein the unit wobble signal is alternatively one of at least four different unit wobble signals and has N carriers, and

wherein a first portion of the unit wobble signal is modulated by using a first modulation method and a second portion of the unit wobble signal is modulated by using a second modulation method.

2.- 4. **(Cancelled)**

5. **(Currently Amended)** The method of claim 1, wherein the ~~generation-generating~~ of the ~~first-unit modulated-wobble~~ signal comprises generating at least two pattern signals indicating at least two-bit values of the coded address data using the first modulation

~~technique~~method, and ~~generating the second modulated signal using the first modulation technique by~~ generating at least two signals used to distinguish signals indicating a bit value of the address data using the second modulation ~~technique~~method, where the coded address data of at least two bits is indicated by disposing ~~the~~ at least two pattern signals in predetermined locations and inserting ~~the~~ at least two signals to distinguish signals indicating a bit value of the address data between the at least two pattern signals.

6. **(Currently Amended)** The method of claim 12, wherein the ~~generation~~generating of the unit wobble signal comprises disposing the first portion of the unit wobble signal and ~~the second modulated signals~~portion of the unit wobble signal adjacent to each other.

7. **(Currently Amended)** The method of claim 12, wherein the ~~generation~~generating of the unit wobble signal comprises alternating the first portion of the unit wobble signal and ~~the second modulated signals~~portion of the unit wobble signal.

8. **(Currently Amended)** The method of claim 14, further comprising:
generating signals indicating each bit of the coded address data.

9. **(Currently Amended)** The method of claim 12, further comprising:
generating a signal indicating a start of the coded address data using one of the first modulation method, and ~~the second modulation technique~~method, and a third modulation ~~technique~~method.

10.-12. **(Cancelled)**

13. **(Currently Amended)** The method of claim 12, wherein the first modulation ~~technique~~method is binary phase shift keying (BPSK), and the second modulation ~~technique~~method is frequency shift keying (FSK).

14.-16. **(Cancelled)**

17. **(Currently Amended)** An apparatus to reproduce a unit wobble signal of a coded address data of a disc-type recording medium, the apparatus comprising:
an optical pick-up reading the unit wobble signal; and
a controller determining that the read unit wobble signal is any one among at least four

different unit wobble signals,

wherein the unit wobble signal is alternatively one of at least four different unit wobble signals and has N carriers, and

wherein a first portion of the unit wobble signal is modulated by using a first modulation method and a second portion of the unit wobble signal is modulated by using a second modulation method.~~An apparatus to modulate address data of a disc-type recording medium, the apparatus comprising:~~

~~an address data generating unit generating the address data;~~

~~an error correction coding unit performing error correction coding of the address data received from the address data generating unit and outputting coded address data;~~

~~a modulating unit generating a first modulated signal of the coded address using a first modulation technique and a second modulated signal of the coded address using a second modulation technique, after receiving the coded address data in a unit of at least two bits from the error correction coding unit; and~~

~~a wobble signal generating unit generating a unit wobble signal by synthesizing the first and second modulated signals received from the modulating unit.~~

18.-20. (Cancelled)

21. (Currently Amended) The apparatus of claim 17, wherein the modulating unit further comprises:

~~a first modulator generating the first modulated signal~~the first portion of the unit wobble signal is modulated using the first modulation technique ~~method~~ by generating at least two pattern signals indicating at least two-bit values of the coded address data; and

~~a second modulator generating the second modulated signal~~the second portion of the unit wobble signal is modulated using the second modulation technique ~~method~~ by generating at least two signals to distinguish signals indicating a bit value of the address data; and

~~wherein, the coded address data of at least two bits is indicated by disposing the~~ at least two pattern signals in predetermined locations and inserting the at least two signals to distinguish the signals indicating a bit value of the address data between the at least two pattern signals.

22. (Currently Amended) The apparatus of claim 17, wherein the wobble signal generating unit generates the unit wobble signal by disposing the first portion of the unit wobble

signal and the second modulated portion of the unit wobble signals are adjacent to each other.

23. **(Currently Amended)** The apparatus of claim 1718, wherein the wobble signal generating unit generates the unit wobble signal by alternating the first portion of the unit wobble signal and the second modulated portion of the unit wobble signals are alternated.

24. **(Currently Amended)** The apparatus of claim 1720, wherein the second modulator modulation method generates signals indicating each bit of the coded address data.

25. **(Currently Amended)** The apparatus of claim 1718, wherein the first modulator generates a signal indicating a start of the coded address data is generated using one of the first modulation method, and the second modulation techniques method, and a third modulation technique method.

26.-28. **(Cancelled)**

29. **(Currently Amended)** The apparatus of claim 1718, wherein the first modulation technique method is a binary phase shift keying (BPSK) and the second modulation technique method is a frequency shift keying (FSK).

30.-32. **(Cancelled)**

33. **(Withdrawn)** A method to demodulate address data of a disc type recording medium, the method comprising:

after receiving a unit wobble signal indicating the address data of at least two bits, which is generated by a synthesizing signal modulated by using first and second modulation techniques, demodulating using the first demodulation technique the signal modulated by the first modulation technique into data of the at least two bits, and demodulating using the second demodulation technique the signal modulated using the second modulation technique into the data of the at least two bits;

determining the address data based on the data demodulated by using the first and second demodulation techniques;

if values of the data of the at least two bits demodulated by using the first and second demodulation techniques are different from each other, generating an eraser flag signal

indicating mismatched bit positions; and

outputting the address data after performing error correction decoding on the address data and after generating the eraser flag signal.

34. **(Withdrawn)** The method of claim 33, further comprising:

performing the demodulation using the first demodulation technique of the signal modulated by using the first modulation technique into a first bit value of the address data, if a predetermined pattern signal exists;

demodulating using the second demodulation technique, the signal modulated by using the first modulation technique into a second bit value of the address data, if the predetermined pattern signal does not exist; and

demodulating using the second demodulation technique each bit value of the signal modulated by using the second modulation technique.

35. **(Withdrawn)** The method of claim 33, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

36. **(Withdrawn)** The method of claim 34, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

37. **(Withdrawn)** An apparatus to demodulate address data of a disc type recording medium, the apparatus comprising:

a demodulating unit, after receiving a unit wobble signal indicating the address data of at least two bits generated by synthesizing signals modulated by first and second modulation techniques, demodulating using the first demodulation technique, the signal modulated by using the first modulation technique into data of the at least two bits, and demodulating using the second demodulation technique the signal modulated by using the second modulation technique into data of the at least two bits;

a data determining unit determining the address data based on the data demodulated by using the first and second demodulation techniques and generates an eraser flag signal indicating mismatched bit positions if values of the data demodulated by using the first and second demodulation techniques are different from each other; and

an error correction decoding unit performing error correction decoding of the determined address data and the eraser flag signal.

38. **(Withdrawn)** The apparatus of claim 37, the demodulating unit comprises:
a first demodulator demodulating the data using the first demodulation technique; and
a second demodulator demodulating the data using the second demodulation technique.

39. **(Withdrawn)** The apparatus of claim 37, wherein the demodulating unit comprises:
a first demodulator demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into a first bit value of the address data, if a predetermined pattern signal exists, and demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into a second bit value of the address data if the predetermined pattern signal does not exist; and
a second demodulator demodulating, using the second demodulation technique, each bit value of the signal modulated by using the second modulation technique.

40. **(Withdrawn)** The apparatus of claim 37, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

41. **(Withdrawn)** The apparatus of claim 38, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

42. **(Withdrawn)** The apparatus of claim 39, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

43. **(Currently Amended)** A computer readable storage medium controlling a computer and having recorded thereon address data modulated by a process of:
generating the address data;
performing error correction coding of the address data and outputting coded address data;
receiving the coded address data in a unit of at least two bits; and

~~generating a first modulated signal of the coded address data using a first modulation technique;~~

~~generating a second modulated signal of the coded address data using a second modulating signal; and~~

~~generating a unit wobble signal of the coded address data, by synthesizing the first and second modulated signals.~~

~~wherein the unit wobble signal is alternatively one of at least four different unit wobble signals and has N carriers, and~~

~~wherein a first portion of the unit wobble signal is modulated by using a first modulation method and a second portion of the unit wobble signal is modulated by using a second modulation method.~~

44.-46. (Cancelled)

47. **(Currently Amended)** The computer readable storage medium of claim 43, wherein the ~~generation-generating~~ of the first modulated unit wobble signal comprises generating at least two pattern signals indicating at least two-bit values of the coded address data using the first modulation technique ~~method~~, and ~~generating the second modulated signal using the first modulation technique by~~ generating at least two signals used to distinguish signals indicating a bit value of the address data using the second modulation technique ~~method~~, where the coded address data of at least two bits is indicated by disposing the at least two pattern signals in predetermined locations and inserting the at least two signals to distinguish signals indicating a bit value of the address data between at least two pattern signals.

48. **(Currently Amended)** The computer readable storage medium of claim 4344, wherein the ~~generation-generating~~ of the unit wobble signal comprises disposing the first portion of the unit wobble signal and the second modulated portion of the unit wobble signals adjacent to each other.

49. **(Currently Amended)** The computer readable storage medium of claim 4344, wherein the ~~generation-generating~~ of the unit wobble signal comprises alternating the first portion of the unit wobble signal and the second modulated signals portion of the unit wobble signal.

50. **(Currently Amended)** The computer readable storage medium of claim 4346, further comprising:

generating signals indicating each bit of the coded address data.

51.-58. **(Cancelled)**

59. **(Withdrawn)** A computer readable recording medium to demodulate address data of a disc type recording medium, comprising:

a demodulating unit, after receiving a unit wobble signal indicating the address data of at least two bits generated by synthesizing signals modulated by first and second modulation techniques, demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into data of the at least two bits, and demodulating, using the second demodulation technique, the signal modulated by using the second modulation technique into data of the at least two bits;

a data determining unit determining the address data based on the data demodulated by using the first and second demodulation techniques and generates an eraser flag signal indicating mismatched bit positions if values of the data demodulated by using the first and second demodulation techniques are different from each other; and

an error correction decoding unit performing error correction decoding of the determined address data and the eraser flag signal.

60. **(Withdrawn)** The computer readable recording medium of claim 59, the demodulating unit comprises:

a first demodulator demodulating the data using the first demodulation technique; and
a second demodulator demodulating the data using the second demodulation technique.

61. **(Withdrawn)** The computer readable recording medium of claim 59, wherein the demodulating unit comprises:

a first demodulator demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into a first bit value of the address data, if a predetermined pattern signal exists, and demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into a second bit value of the address data if the predetermined pattern signal does not exist; and

a second demodulator demodulating using the second demodulation technique each bit

value of the signal modulated by using the second modulation technique.

62. **(Withdrawn)** The apparatus of claim 37, wherein the BPSK and FSK pattern signals alternate in the unit wobble signal.

63. **(Withdrawn)** The apparatus of claim 37, wherein the start of the address data of the at least two bits is indicated by using BPSK signals indicating the bit value "0" or "1" of the address data of the at least two bits.

64. **(New)** The method of claim 1, wherein N is 56.

65. **(New)** The method of claim 1, wherein the unit wobble signal comprises 2 bits.

66. **(New)** The method of claim 17, wherein N is 56.

67. **(New)** The method of claim 17, wherein the unit wobble signal comprises 2 bits.

68. **(New)** The method of claim 43, wherein N is 56.

69. **(New)** The method of claim 43, wherein the unit wobble signal comprises 2 bits.